**БЕЛОРУССКИЙ ГОСУДАРСТВЕННЫЙ УНИВЕРСИТЕТ**

**ИНФОРМАТИКИ и РАДИОЭЛЕКТРОНИКИ**

**Факультет компьютерных систем и сетей**

**Кафедра ЭВМ**

Контроль и диагностика средств вычислительной техники

Лабораторная работа № 2

Тестирование элементов памяти на уровне поведения.

Тесты КМОП-структур на переключательном уровне

Вариант №7

**Выполнил: Проверил:**

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**Пашковский А.А.**

**Минск 2016**

**Триггер**: D-триггер со сбросом и установкой.



Таблица функционирования

D-триггера со сбросом и установкой

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| R | S | D | C | Q |
| 1 | - | - | 0 | 0 |
| 0 | 1 | - | 0 | 1 |
| 0 | 0 | - | 1 | (D) |
| 0 | 0 | - | 0 | N |

Функциональный тест построенный на базе таблицы функционирования:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| R | S | D | C | Q | Операция |
| 1 | 0 | 0 | 0 | 0 | Сброс в 0 |
| 0 | 0 | 1 | 1 | 1 | Установка 1 |
| 0 | 0 | 1 | 0 | 1 | Хранение 1 |
| 0 | 0 | 0 | 1 | 0 | Установка 0 |
| 0 | 0 | 0 | 0 | 0 | Хранение 0 |
| 0 | 0 | 1 | 1 | 1 | Установка 1 |
| 1 | 0 | 1 | 0 | 0 | Сброс в 0 |
| 0 | 0 | 0 | 1 | 0 | Установка 0 |
| 0 | 1 | 0 | 0 | 1 | Установка 1 |

Код схемы на VLSI-SIM:

circuit trigger;

inputs R(1), S(1), D(1), C(1);

outputs Q(1);

GATES

NC 'NOT'(1) C(1);

NNC 'NOT'(1) NC(1);

NS 'NOT'(1) S(1);

NOA22\_R 'NOA22'(1) NOA2\_R(1),NC(1),D(1),NNC(1);

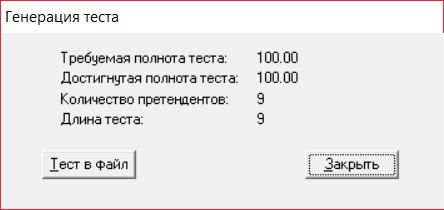
NOA2\_R 'NOA2'(1) R(1),NOA22\_R(1),NS(1);

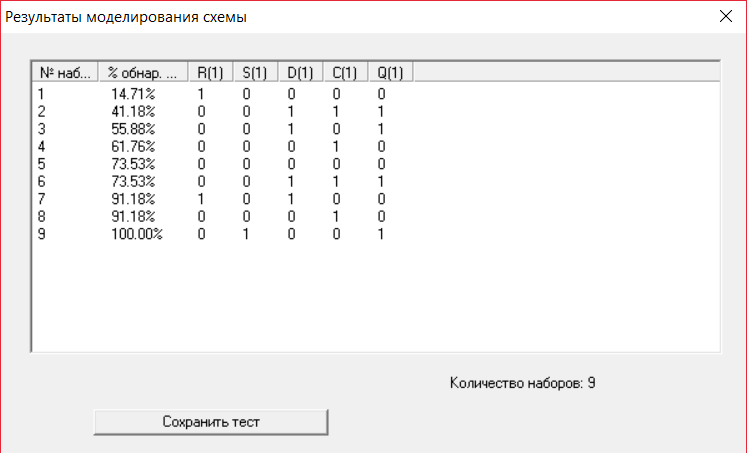
Q 'NOT'(1) NOA22\_R(1);

ENDGATES

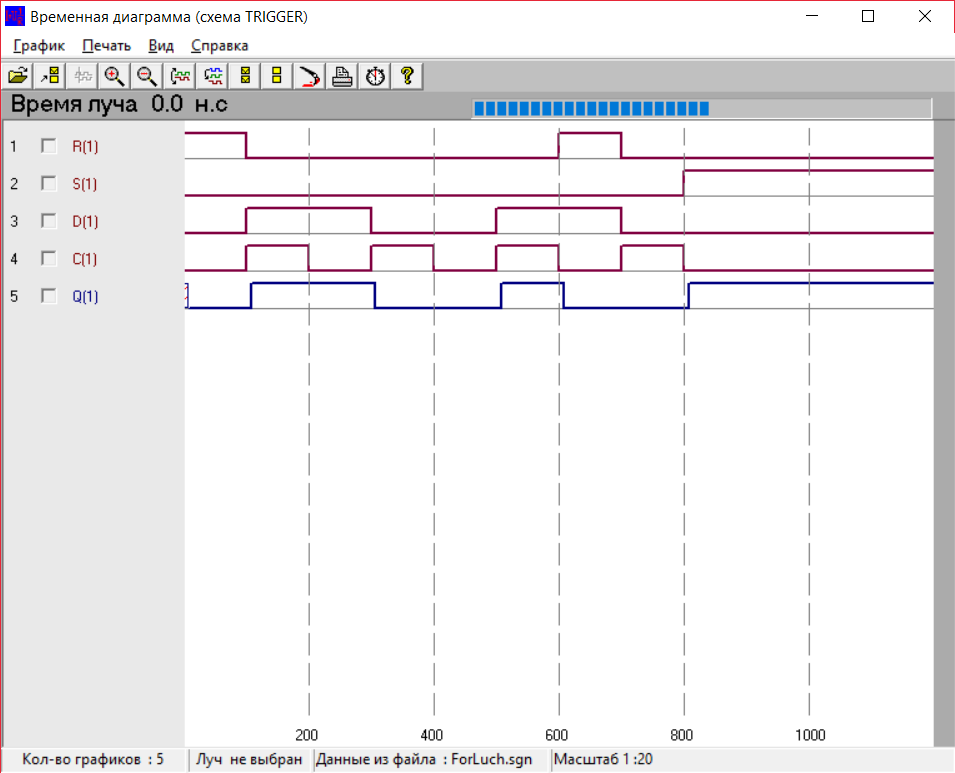
END

**Определение контролирующей способности функционального теста:**

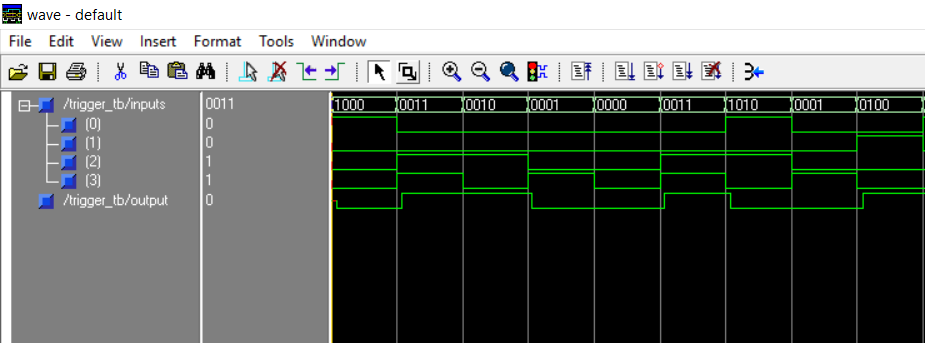




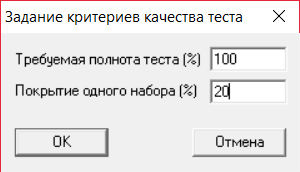
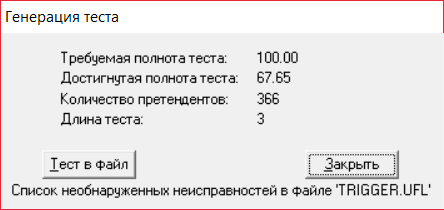
Моделирование на функциональном наборе (VLSI-SIM):

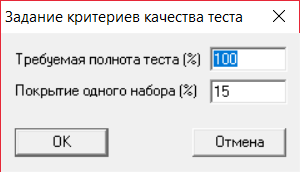
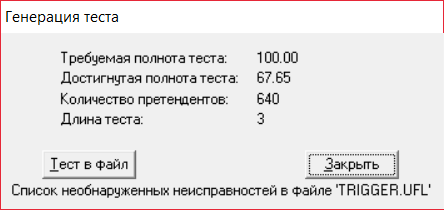


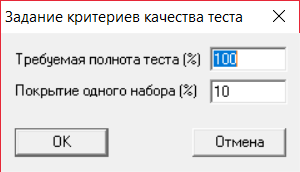
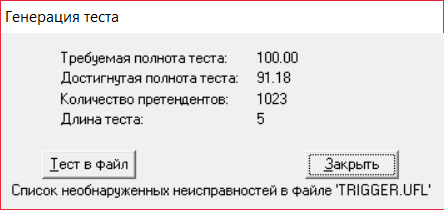
Моделирование на функциональном наборе (MODEL-SIM):

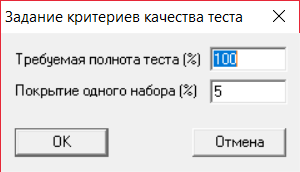
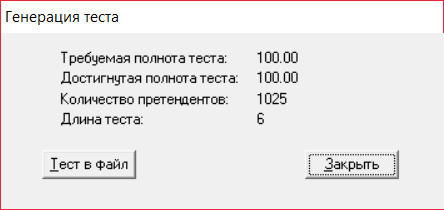


**Построение автоматического теста:**

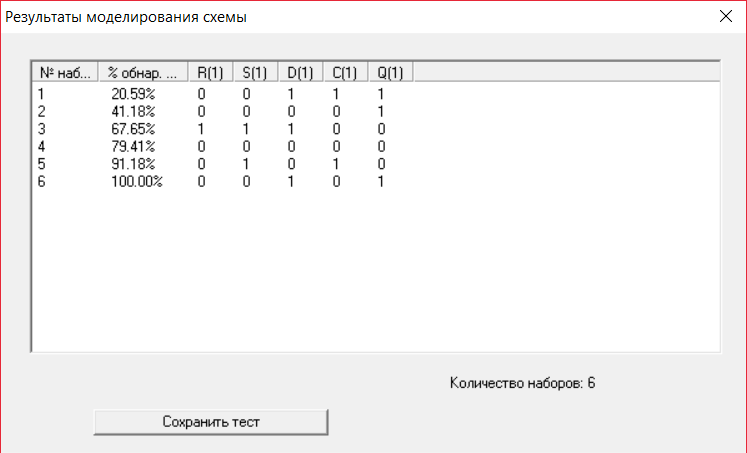




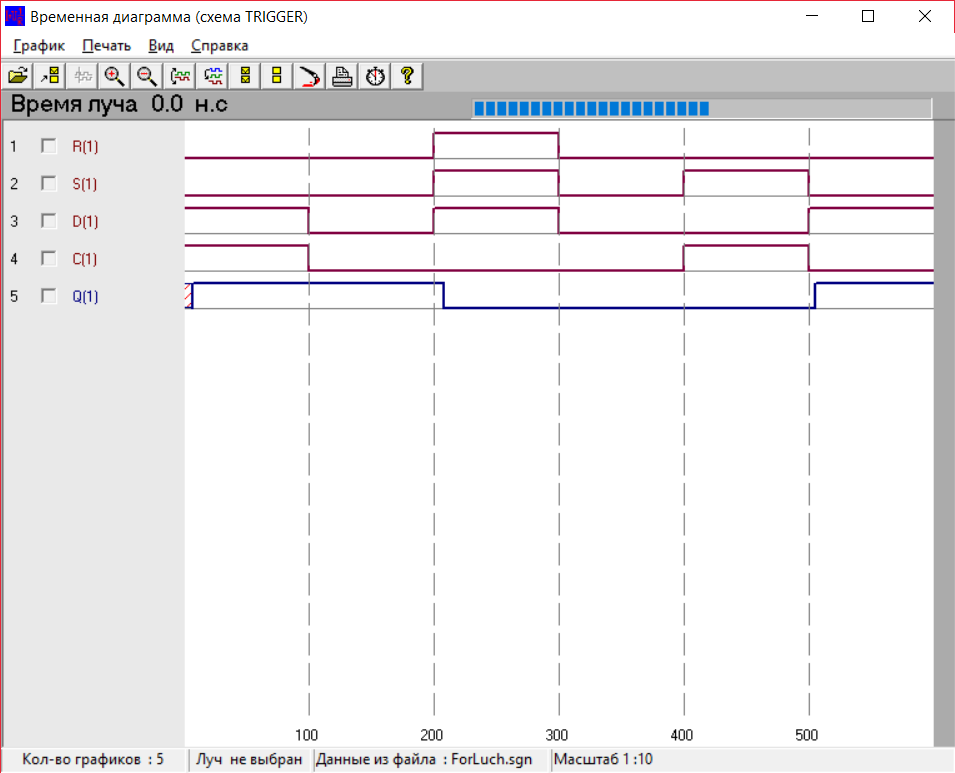




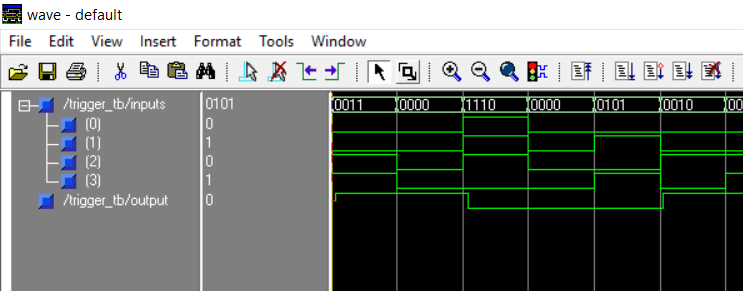
Результат построения автоматического теста:



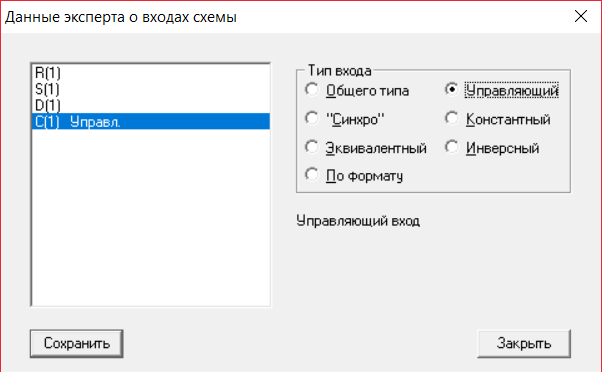
Моделирование на автоматическом тесте (VLSI-SIM):

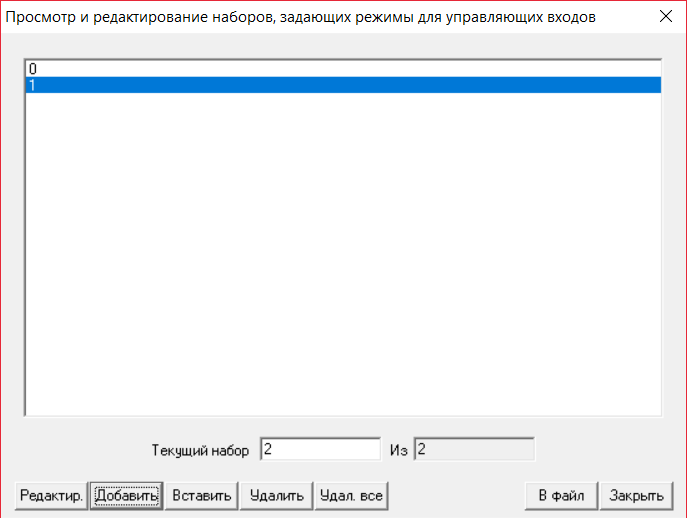


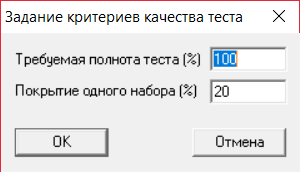
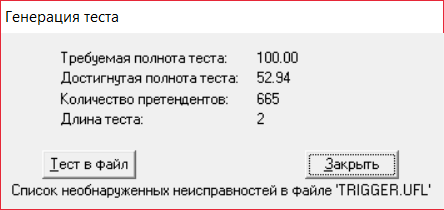
Моделирование на автоматическом тесте (MODEL-SIM):

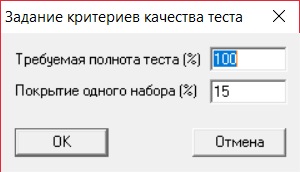
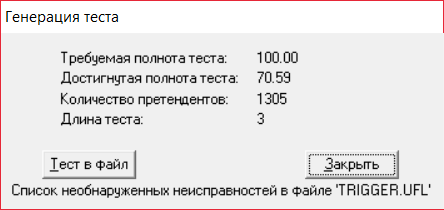


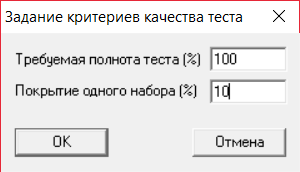
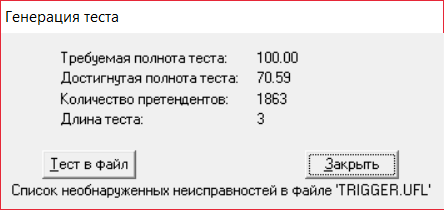
**Построение автоматизированного теста:**

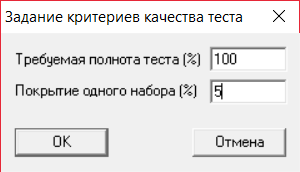
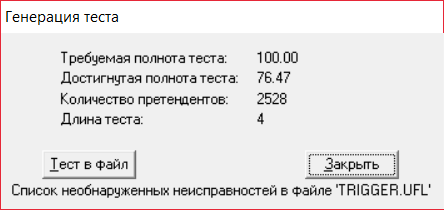


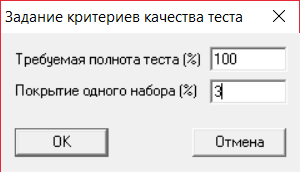
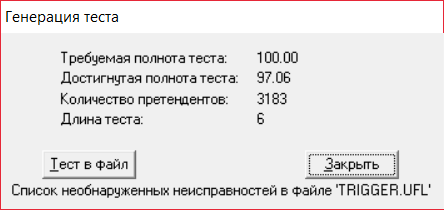


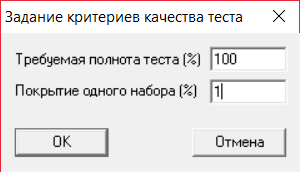
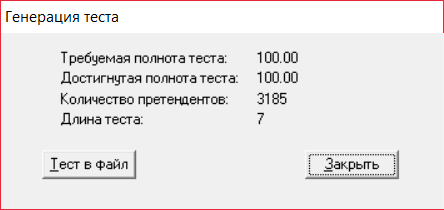




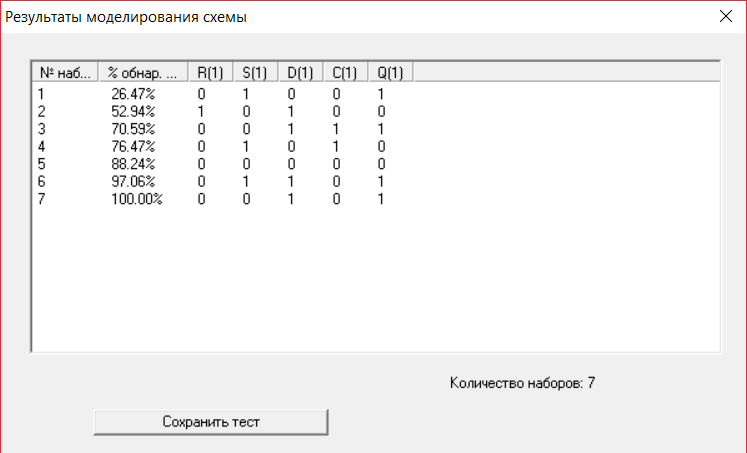




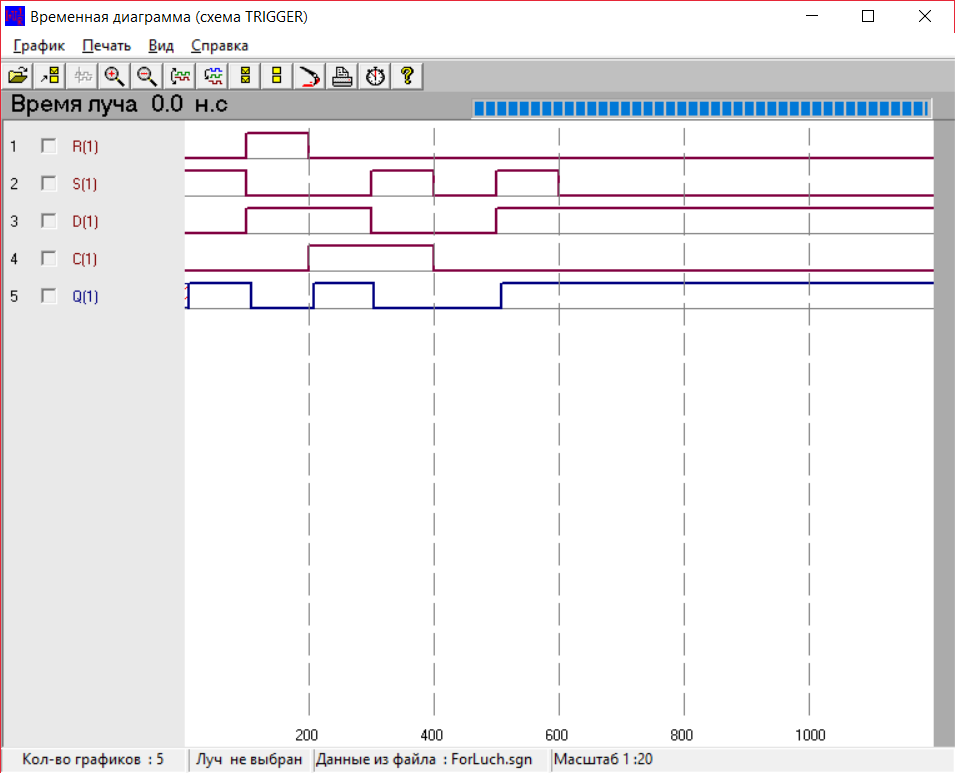




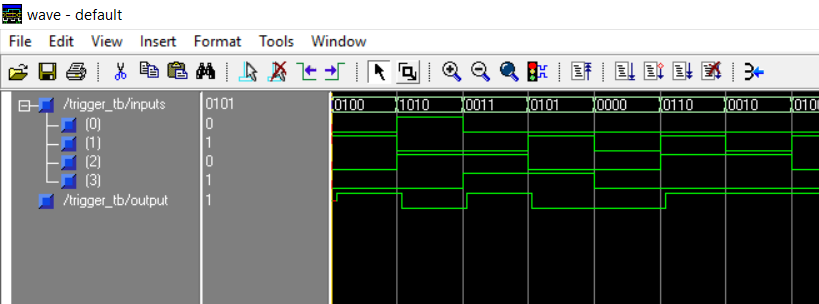
Результат:



Моделирование на автоматизированном тесте (VLSI-SIM):



Моделирование на автоматизированном тесте (MODEL-SIM):



Исходный код схемы на VHDL:

Элемент N:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity N is

Port (

INPUT: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end N;

architecture Behavioral of N is

begin

OUTPUT <= not INPUT after 1 ns;

end Behavioral;

Элемент NOA:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity NOA is

Port (

A: in STD\_LOGIC;

B: in STD\_LOGIC;

C: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end NOA;

architecture Behavioral of NOA is

begin

OUTPUT <= not(A or (B and C))after 3 ns;

end Behavioral;

Элемент NOAA:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity NOAA is

Port (

A: in STD\_LOGIC;

B: in STD\_LOGIC;

C: in STD\_LOGIC;

D: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end NOAA;

architecture Behavioral of NOAA is

begin

OUTPUT <= not((A and B) or (C and D)) after 4 ns;

end Behavioral;

Структурная схема триггера:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity trigger is

Port (

D: in STD\_LOGIC;

R: in STD\_LOGIC;

S: in STD\_LOGIC;

C: in STD\_LOGIC;

Q: out STD\_LOGIC

);

end trigger;

architecture Behavioral of trigger is

component N

Port (

INPUT: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end component;

component NOA

Port (

A: in STD\_LOGIC;

B: in STD\_LOGIC;

C: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end component;

component NOAA

Port (

A: in STD\_LOGIC;

B: in STD\_LOGIC;

C: in STD\_LOGIC;

D: in STD\_LOGIC;

OUTPUT: out STD\_LOGIC

);

end component;

signal ns, nc, nnc: STD\_LOGIC;

signal noaa\_r, noa\_r: STD\_LOGIC;

begin

n\_first\_instance: N port map(C, nc);

n\_second\_instance: N port map(nc, nnc);

n\_third\_instance: N port map(S, ns);

noaa\_first\_instance: NOAA port map(noa\_r, nc, D, nnc, noaa\_r);

noa\_first\_instance: NOA port map(R, ns, noaa\_r, noa\_r);

n\_four\_instance: N port map(noaa\_r, Q);

end Behavioral;

Поведенческая схема триггера:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity trigger\_behavioral is

Port (

D: in STD\_LOGIC;

R: in STD\_LOGIC;

S: in STD\_LOGIC;

C: in STD\_LOGIC;

Q: out STD\_LOGIC

);

end trigger\_behavioral;

architecture Behavioral of trigger\_behavioral is

begin

process (D, R, S, C)

variable trigger\_state: STD\_LOGIC := '0';

begin

if (R = '1' and C = '0') then

trigger\_state := '0';

Q <= trigger\_state;

end if;

if (R = '0' and S = '1' and C = '0') then

trigger\_state := '1';

Q <= trigger\_state;

end if;

if (R = '0' and S = '0' and C'event and C = '1') then

trigger\_state := D;

Q <= trigger\_state;

end if;

if (R = '0' and S = '0' and C = '0') then

Q <= trigger\_state;

end if;

end process;

end Behavioral;

Тест:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity trigger\_tb is

--Port ( );

end trigger\_tb;

architecture Behavioral of trigger\_tb is

component trigger

Port (

D: in STD\_LOGIC;

R: in STD\_LOGIC;

S: in STD\_LOGIC;

C: in STD\_LOGIC;

Q: out STD\_LOGIC

);

end component;

type TRIGGER\_TEST is array (natural range <>) of STD\_LOGIC\_VECTOR(0 to 3);

signal inputs: STD\_LOGIC\_VECTOR(0 to 3);

signal output: STD\_LOGIC;

constant manual\_functional\_test: TRIGGER\_TEST(0 to 8) := (

"1000",

"0011",

"0010",

"0001",

"0000",

"0011",

"1010",

"0001",

"0100"

);

constant automatic\_functional\_test: TRIGGER\_TEST(0 to 5) := (

"0011",

"0000",

"1110",

"0000",

"0101",

"0010"

);

constant automatization\_functional\_test: TRIGGER\_TEST(0 to 6) := (

"0100",

"1010",

"0011",

"0101",

"0000",

"0110",

"0010"

);

begin

trigger\_instance: trigger port map(

R => inputs(0),

S => inputs(1),

D => inputs(2),

C => inputs(3),

Q => output

);

process

begin

for index in 0 to 6 loop

inputs <= automatization\_functional\_test(index);

wait for 100ns;

end loop;

end process;

end Behavioral;

Построение тестов контроля в классе неисправностей ПЗТ:

7 Комбинационный элемент 2И-3ИЛИ-НЕ (NO3A2)

